IN THE CLAIMS

Please enter the below claim amendments.

1. (Currently Amended) A method comprising:

receiving an address comprising of a logical chip select vector for at least one memory module;

converting the logical chip select vector to a corresponding physical chip select vector associated with a physical location of the at least one memory module that is different than the logical chip select vector; and

accessing the memory module using the physical chip select vector, wherein converting the logical chip select vector to the physical chip select vector, comprises:

determining at least one index from the logical chip select (CS) vector; and

retrieving a physical chip select vector associated with the index from a table comprising a plurality of physical chip select vectors.

2. (Cancelled)

3. (Currently Amended) The method of claim 21, wherein converting the address of the logical chip select vector to the physical chip select vector, further comprises:

mapping the physical chip select vector to a first memory module; and

mapping the physical chip select vector to a second memory module

4. (Currently Amended) The method of claim 1, wherein the memory module is a dual in-line memory module (DIMM).

5. (Previously Presented) The method of claim 1, wherein the memory module is a dynamic access random access memory (DRAM)

6. (Currently Amended) A system, comprising:

a memory controller operable to generate a logical chip select vector based on a one-to-one relationship between a memory map and a plurality of memory modules;

at least one physical chip select vector ~~physically connected to at least one of~~ corresponding to the plurality of memory modules;

a chip select remapping unit operable to convert the logical chip select vector ~~based~~ to a physical chip select vector,

wherein the physical chip select vector is operable to allow the memory controller to access memory modules, wherein the chip select remapping unit comprises:

an index conversion unit operable to generate at least one index based on the logical chip select vector; and

a table comprising a plurality of physical chip select vectors, wherein each physical chip select vector is associated with at least one index and identifies the physical location of at least one memory module.

7. (Previously Presented) The system of claim 6, further comprising a central processing unit operable to instruct the memory controller to access at least one of the memory modules.

8. (Cancelled)

9. (Currently Amended) The system of claim 6, wherein the chip select remapping unit is further operable to:

use the physical chip select vector to map the logical chip select vector to a first memory module ~~using~~; and

use the physical chip select vector to map the logical chip select vector to a second memory module.

10. (Previously Presented) The system of claim 9, wherein the memory module is a dual in-line memory module (DIMM).

11. (Previously Presented) A chip select remapping unit, comprising:

an index conversion unit operable to generate at least one index based on a logical chip select vector; and

a table comprising a plurality of physical chip select vectors, wherein each physical chip select vector is associated with at least one index and identifies a physical location of at least one memory module.

12. (Previously Presented) The chip select remapping unit of claim 11, further operable to:

map the physical chip select vector to a first memory module; and

map the physical chip select vector to a second memory module

13. (Previously Presented) The chip select remapping unit of claim 11, wherein the at least one memory module is a dual in-line memory modules (DIMMs).

14. (Cancelled)

15. (Cancelled)